dent of the choice of w provided we choose w great enough, say $w \geq 16$. A change in S will basically move the curves only up and down; it will not affect the positions of their minima.

We notice again that increasing the bit size will decrease the optimal choice of α. Comparing Figs. 6 and 10 we see that content addressable memories should have smaller branching ratios than random-access memories. For $b_1 = 4$, which seems a reasonable figure, the optimal choice of α is 4.

V. Conclusion

We have presented a general method for analyzing the cost and performance of recursively defined VLSI structures. Parameters of any such structure may be optimized with respect to time, area, or some combination of the two. While we have chosen the area-time product, it is clear that some other choice may be appropriate for any given application.

The results of this study indicate that as more processing is available in each module at level zero, the optimal value of α will decrease. A system with $\alpha = 4$ would seem to be appropriate for memories in which substantial processing is comingled with storage.

Very general arguments were used to generate the basic recursive structure. For that reason it appears that a very large fraction of VLSI computing structures will be designed in this way. We have discussed two examples, one in which the basic elements were bits of storage, and one with words of storage at the lowest level. They gave rise to rather different recursive structures. The way in which their area and time measures were established should make it clear how to apply these techniques to other recursively defined computing structures.

Carver A. Mead, for a biography and photograph, see this issue, p. 470.

Martin Rem was born in The Netherlands on September 22, 1946. He received the B.S. degree in mathematics and physics and the M.S. degree in mathematics from the University of Amsterdam, Holland, in 1968 and 1971, respectively, and the Ph.D. degree in computer science from Eindhoven University of Technology, Eindhoven, The Netherlands, in 1976.

He is an Associate Professor of Mathematics in the Department of Mathematics, Eindhoven University of Technology. He is presently a Visiting Professor of Computer Science in the Department of Computer Science, California Institute of Technology, Pasadena, CA. His major research interests are in the area of programming of machines with in-store processing, semantics of programming languages, correctness proofs, and well-structured machine designs.

Dr. Rem is a member of the Association for Computing Machinery, the Dutch Computer Society NGI, and the Dutch Mathematical Society.

Delay-Time Optimization for Driving and Sensing of Signals on High-Capacitance Paths of VLSI Systems

AMR M. MOHSEN, MEMBER, IEEE, AND CARVER A. MEAD

Abstract—**Transmission of signals on large capacitance paths in a VLSI system may result in substantial degradation of the overall system performance. In this paper minimization of the delay times associated with driving and sensing signals from large capacitance paths by optimizing the fan-out factor of the driver stages, the gain of the input sensing stages, and the path voltage swing are examined. Examples of driving signals on a high capacitance path with two driving schemes are: a push-pull depletion-load driver chain and a fixed driver; and of sensing signals with two sensing schemes: a single-ended depletion-load inverter input stage and a balanced regenerative strobed latch are presented. We conclude that minimum delay time is achieved when the delay times of the successive stages of the driver chain, the high capacitance path, and the input sensing stage are comparable. In general, transmission time of signals in a system is minimized when the delay times of the different stages of the system are comparable.**

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I. Introduction

THE OVERALL PERFORMANCE of VLSI systems may be seriously degraded if signals need to be transmitted from one part to other parts in the system across large capacitance paths [1]. This large fan-out situation often occurs in the case of control drivers that are required to drive a large number of inputs to memory cells or logic-function blocks across a chip, or in the case of sensing stored information from small cells of large memory arrays. A similar and even more serious problem is driving wires which go off the silicon chip to other chips or input and output devices. In such cases, the

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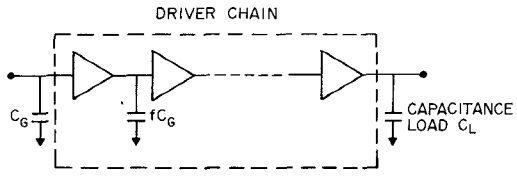

Fig. 1. Driver chain driving a high capacitance load C_L.

ratio of the capacitance that must be driven to the inherent capacitance of a gate circuit on the chip is often many orders of magnitude, causing a serious delay and degradation of system performance.

In this paper we examine, in general terms, optimum means of minimizing the delay time associated with transmitting information on large capacitance paths. In Section II, we analyze the driving of capacitive loads in the minimum possible time. In Section III, we examine the driving and sensing circuits with minimum possible delay times. In Section IV, we consider the sensing of signals on large capacitance lines driven by fixed sources. The general guidelines for designing the driver and sensing circuits of signals on high capacitance paths for minimum delay time are summarized in Section IV.

II. Driving Large Capacitive Loads

Consider how we may drive a capacitive load C_L in the minimum possible time. Let us assume we are starting with a signal V_i at the input of an elementary driver of input capacitance C_G. The elementary driver can be a simple static inverter or a dynamic clocked driver. Define the ratio of the load capacitance to the input capacitance C_L/C_G as Y. It seems intuitively clear that the optimum way to drive a large capacitance is to use the elementary driver to drive a larger driver and that larger driver to drive a still larger driver until at some point the larger driver is able to drive the load capacitance directly, as shown in Fig. 1. Let the delay time associated with the elementary driver driving a similar driver be τ_{Dr}. Thus the delay associated with the elementary driver driving a larger driver by a factor f is $f\tau_{Dr}$. If N such stages are used, each larger than the previous by a factor f, then the total delay of the driver chain τ_{ch} is given by

$$\tau_{ch} = Nf\tau_{Dr}. \tag{1}$$

Also, the capacitance ratio Y is related to N and f by

$$Y = f^N, \quad \ln Y = N \ln f. \tag{2}$$

Substituting (2) into (1)

$$\tau_{ch} = \ln Y \cdot \left[\frac{f}{\ln f}\right] \tau_{Dr}. \tag{3}$$

Thus the total delay is always proportional to $\ln Y$ as a result of the exponential growth in successive stages of the driver. The multiplicative factor $f/\ln(f)$ is plotted as a function of f in Fig. 2 normalized to its minimum value e. Total delay time is minimized when each stage is larger than the previous one by a factor of e, the base of natural logarithms. Minimum total delay $\tau_{ch/min}$ is given by

$$\tau_{ch/min} = \tau_{Dr} e \ln\left(\frac{C_L}{C_G}\right). \tag{4}$$

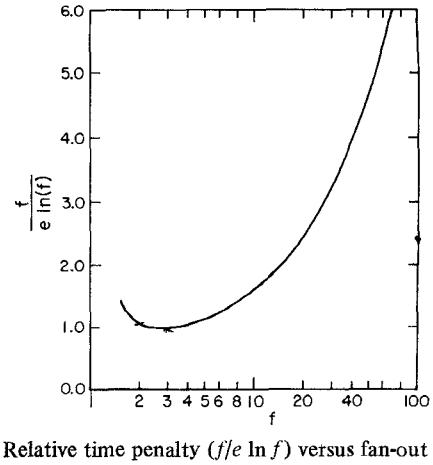

Fig. 2. Relative time penalty ($f/e \ln f$) versus fan-out factor f.

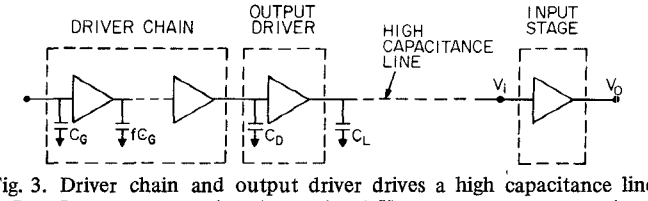

Fig. 3. Driver chain and output driver drives a high capacitance line C_L. Input stage receives input signal V_i to generate output voltage V_o.

The minimum of the driver-chain delay in Fig. 2 is rather broad with a relatively small delay-time penalty for fan-out factor f above e.

III. Driving and Sensing Signals on Large Capacitance Lines

Consider how we may minimize the time to transfer a signal through a high capacitance line by optimizing the driver circuit at one end of the line and the input sensing circuit at the other end of the line. It has been shown previously that a driver chain can be optimized to minimize the delay time required to drive the line capacitance C_L. We will consider below the implications of optimizing the input sensing circuit with the driver circuit by examining the effect of the gain of the input stage and the line voltage swing on the total delay time of signal transmission on the high capacitance path.

In Fig. 3 the driver is made of a driver chain as described in Section II, where the voltage swing is equal to the supply voltage, and an output driver that drives the large capacitance line with a voltage swing equal to V_i. The input stage senses the signal at the other end of the line and generates an output voltage V_o equal to the supply voltage. The input stage can be a single-ended circuit or a differential regenerative or nonregenerative circuit. The gain of the input stage G is defined as

$$G = \frac{V_o}{V_i}. \tag{5}$$

The delay associated with the input stage sensing τ_i is a function of the input voltage swing V_i required to generate V_o at the output, i.e., it is a function of the input-stage gain

$$\text{Input-Stage Delay} = \tau_i(V_i). \tag{6}$$

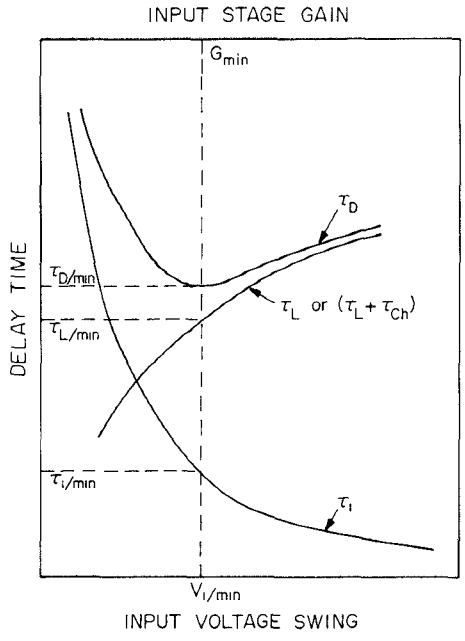

Fig. 4. Delay time of driver stages τ_{ch}, output driver τ_L, and input stage τ_i versus input-stage gain and input voltage swing.

For smaller V_i, the input stage sensing delay τ_i is larger as shown in Fig. 4. The functional relationship can be written as

$$\tau_i(V_i) = \tau_0 f(V_i) \tag{7}$$

where τ_0 is the characteristic transit time of the technology (transit time across the channel in the MOS technology or across the base in the bipolar technology).

The time required for the output driver to charge and discharge the large capacitance line by a voltage V_i is given by

$$\tau_L = \frac{C_L}{I_o} V_i \tag{8}$$

$$\tau_L = \frac{C_L}{I_o}\frac{1}{G} V_o = C_L R_o \frac{1}{G} = \frac{T_0}{G} \tag{9}$$

where

$$R_o = \frac{V_o}{I_o} \quad \text{and} \quad T_0 = C_L R_o. \tag{10}$$

I_o represents the current driving capability of the output driver and is given [1] by

$$I_o = C_D \frac{V_o}{\tau_{Dr}} \tag{11}$$

where C_D is the input capacitance of the output driver. The minimum possible driver-chain delay, as shown in Section II, is given by

$$\tau_{ch} = \tau_{Dr} e \ln \frac{C_D}{C_G}. \tag{12}$$

If the input-stage circuit configuration is such that the input voltage V_i is sampled and it is then clocked to amplify V_i to V_o, the total delay time τ_D is approximately equal to the driver-chain delay τ_{ch} plus the delay associated with driving the large capacitance line τ_L plus the input stage sensing delay τ_i

$$\tau_D = \tau_{ch} + \tau_L + \tau_i. \tag{13}$$

As shown in Appendix A, the above sum previously given still represents approximately τ_D for other input circuit configurations if $\tau_L \gtrsim \tau_i$. Substituting in (13), we get

$$\tau_D = \tau_{Dr} e \ln \frac{C_D}{C_G} + \frac{C_L}{C_D}\tau_{Dr}\frac{V_i}{V_o} + \tau_i(V_i). \tag{14}$$

An optimum value of C_D results by putting the partial derivative $(\partial\tau_D/\partial C_D) = 0$, and is given by

$$C_{D/opt} = \frac{C_L}{e}\frac{V_i}{V_o} = \frac{C_L}{e}\cdot\frac{1}{G}. \tag{15}$$

Substituting in (13),

$$\tau_D = \tau_{Dr} e \ln \frac{C_L}{C_G}\frac{V_i}{V_o} + \tau_i(V_i). \tag{16}$$

The first term in (16) represents the delay in the driver chain τ_{ch} and the output driver τ_L and is less than the delay τ_{ch} in (4), as the signal swing on the output lines is reduced by the gain V_o/V_i. Thus, the optimum output driver delay is equal to the delay per stage of the driver chain. The delay times are plotted in Fig. 4 versus V_i. By equating the partial derivative $(\partial\tau_D/\partial V_i) = 0$, we get the optimum swing $V_{i|min}$ of the line for minimum delay time τ_D

$$\tau_{Dr} e \frac{1}{V_{i|min}} + \frac{\partial\tau_i}{\partial V_i}(V_{i|min}) = 0 \tag{17}$$

which defines $V_{i|min}$ and by substituting in (16) results in the minimum possible delay $\tau_{D|min}$ for transferring a signal on such a high capacitance path.

The input-stage delay τ_i in (6) can be written as a monotonic function of the gain G defined in (5)

$$\tau_i = \tau_0 f\left(\frac{V_o}{G}\right) = \tau_0 g(G). \tag{18}$$

The total delay time in (17) can also be written as a function of the gain G

$$\tau_D = \tau_{Dr} e \ln \frac{C_L}{C_G}\frac{1}{G} + \tau_0 g(G). \tag{19}$$

The dependence of τ_i, $(\tau_{ch} + \tau_L)$ and τ_D on the gain G is illustrated in Fig. 4.

If the input-stage circuit configuration is such that

$$\tau_i = \tau_0 \alpha G^n, \quad n \geqslant 1 \tag{20}$$

then (19) reduces to

$$\tau_D = \tau_{Dr} e \ln \frac{C_L}{C_G}\frac{1}{G} + \tau_0 \alpha G^n. \tag{21}$$

Since the frequency bandwidth (BW) of the input sensing stage is proportional to $1/\tau_i$, (20) can be rewritten as

$$G \cdot \mathrm{BW} = \frac{1}{\tau_0 \alpha G^{n-1}}. \tag{22}$$

Thus the input-stage sensing delay τ_i dependence on the gain G is a reformulation of the gain-bandwidth product of the input

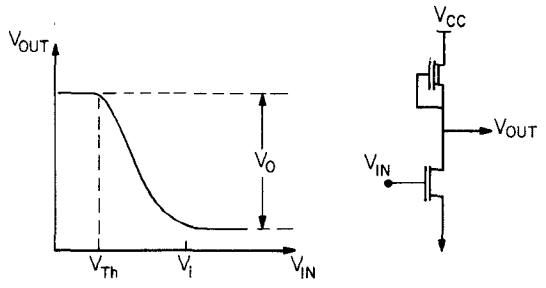

Fig. 5. Depletion-load-inverter input stage.

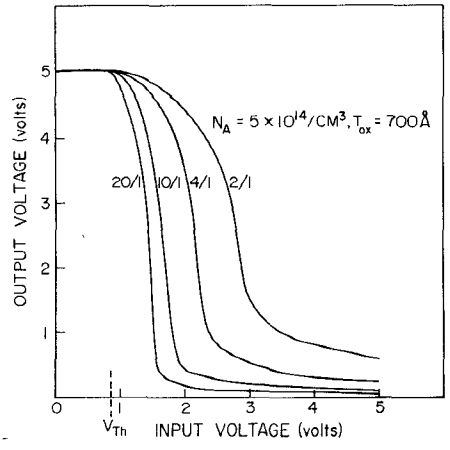

Fig. 6. Input-output voltage characteristics of a depletion-load-inverter input stage for different aspect ratios of the pull-down to pull-up transistors.

stage, which is limited by the characteristic transit time of the technology τ_0. The minimum delay time occurs at

$$G_{i|\min} = \left(\frac{\tau_{Dr} e}{n\alpha\tau_0}\right)^{1/n} \qquad V_{i|\min} = V_o\left(\frac{n\alpha\tau_0}{e\tau_{Dr}}\right)^{1/n}$$

$$\tau_{i|\min} = \frac{e\tau_{Dr}}{n} \tag{23}$$

where $\tau_{i|\min}$ is independent of the ratio of load capacitance to gate capacitance (C_L/C_G). The minimum possible delay $\tau_{D|\min}$ for transferring the signal through the high capacitance path is given by

$$\tau_{D|\min} = \tau_{Dr} e\left[\frac{1}{n} + \ln\frac{C_L}{C_G}\left(\frac{n\alpha\tau_0}{\tau_{Dr} e}\right)^{1/n}\right]. \tag{24}$$

We consider below two numerical examples of a single-ended depletion-load-inverter input stage and a differential regenerative strobed-latched input stage.

A. Depletion-Load-Inverter Input Stage

For the depletion-load MOS inverter input stage in Fig. 5, the input-output characteristics for different aspect ratios are shown in Fig. 6. The gain of the stage is given [2] by

$$\frac{V_o}{V_i - V_{th}} = K\sqrt{r} \tag{25}$$

where r is the aspect ratios of the load and pull-down transistors and K is a constant given by

$$K = \frac{2}{\alpha f}\sqrt{V_Q + V_{BB}}$$

where α is the body factor $= \sqrt{(2eN_A\epsilon_s/C_{0x})}$; V_{BB} is the substate bias; V_Q is the quiescent output voltage $\cong (V_{cc}/2)$; and f is a constant. The input-stage delay is dominated by the rise time of the stage and is given [1] by

$$\tau_i = 4(O+p)\tau_0(r+1) \simeq 4(O+p)\tau_0 r \tag{26}$$

where

- O inverter output fan-out;
- p parasitic to intrinsic gate capacitance;
- τ_0 transit time across gate of pull-down transistor, and is given by

$$\tau_0 = \frac{L}{V_d} \simeq \frac{L^2}{\mu_{eff}(V_G - V_{th})} \tag{27}$$

where

- L gate length of the pull-down transistor;
- V_d carrier drift velocity under the gate;
- μ_{eff} effective carrier mobility;
- $(V_G - V_{th})$ voltage drop across inversion layer in saturation.

Thus the relationship in (6) reduces to

$$\tau_i = \tau_0 \frac{EV_o^2}{(V_i - V_{th})^2} \tag{28}$$

where E is a dimensionless constant equal to $[4(O+p)/K^2]$.

Assuming the voltage swing on the high capacitance path is between V_{th} and V_i, the delay times for the depletion-load-inverter input stage reduce to

$$\tau_{ch} + \tau_L = e\tau_{Dr} \ln\frac{C_L}{C_G}\frac{(V_i - V_{th})}{V_o}$$

$$\tau_i = \tau_0 E \frac{V_o^2}{(V_i - V_{th})^2}$$

$$\tau_D = e\tau_{Dr} \ln\frac{C_L}{C_G}\left(\frac{V_i - V_{th}}{V_o}\right) + \tau_0 E\left(\frac{V_o}{V_i - V_{th}}\right)^2. \tag{29}$$

In Fig. 7 τ_i, $(\tau_{ch} + \tau_L)$ and τ_D are plotted for a depletion-load-inverter input stage with the following parameters: $L = 4$ μm; $\mu_{eff} \cong 500$ cm^2/V · s; $(V_G - V_{th}) \cong 4$ V; $\tau_0 = 1/20$ ns; $O + p = 5$; $k = 3$; and $E = 2.2$. The driver chain consists of depletion-load push-pull buffers with the following parameters: $P = 5$, $\tau_0 = 1/20$ ns; $r = 4$; $\tau_{Dr} = 20$; $\tau_0 = 1$ ns; $C_G = 0.1$ pF; $C_L = 50$ pF; $C_L/C_G = 500$. τ_D has a minimum at

$$(V_i - V_{th})_{\min} = W_o\sqrt{\frac{2\tau_0 E}{e\tau_{Dr}}} \tag{30}$$

where the values of τ_i, $(\tau_{ch} + \tau_L)$, τ_0 and G are given by

$$\tau_{i|\min} = 0.5\,\tau_{Dr} e$$

$$\tau_{ch} + \tau_{L|\min} = e\tau_{Dr} \ln\frac{C_L}{C_G}\sqrt{\frac{2\tau_0 E}{e\tau_{Dr}}}$$

$$\tau_{D|\min} = \tau_{Dr} e\left[0.5 + \ln\frac{C_L}{C_G}\sqrt{\frac{2\tau_0 E}{e\tau_{Dr}}}\right]$$

$$G_{|\min} = \sqrt{\frac{e\tau_{Dr}}{2\tau_0 E}}. \tag{31}$$

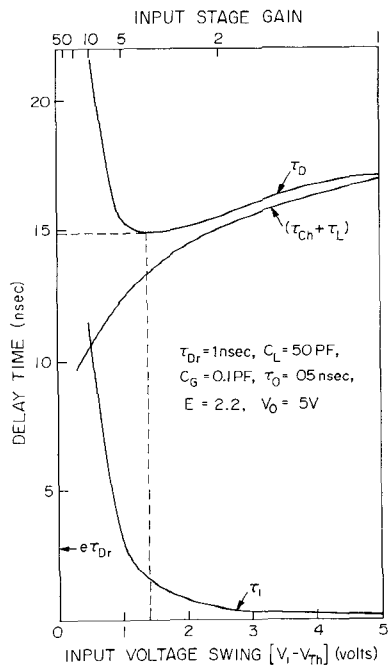

Fig. 7. Delay time versus line voltage swing V_i and input-stage gain G for a depletion-load push-pull driver chain driving 50-pF load and a depletion-load-inverter input stage.

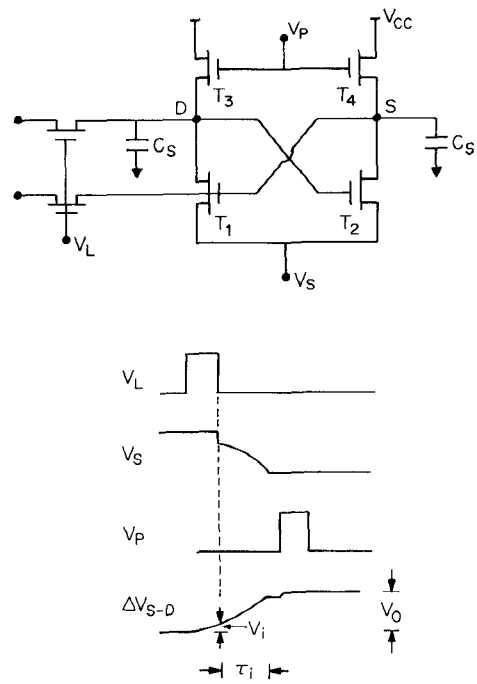

Fig. 8. Regenerative balanced strobed-latch input stage.

In Fig. 7 the delay of the driver chain is the dominant component of the total delay time for input voltage swing $V_1 > 0.8$ V and input-stage gain $G < 8$. The total delay time increases logarithmically with the line voltage swing for line voltage swings above the optimum value. The increase in τ_D by increasing the voltage swing on the high capacitance line from 1.4 to 5 V is only 15 percent. Therefore, in such cases full supply-voltage swing on the high capacitance line provides better immunity against interfering signals with a relatively small delay-time penalty. However, increasing the input-stage

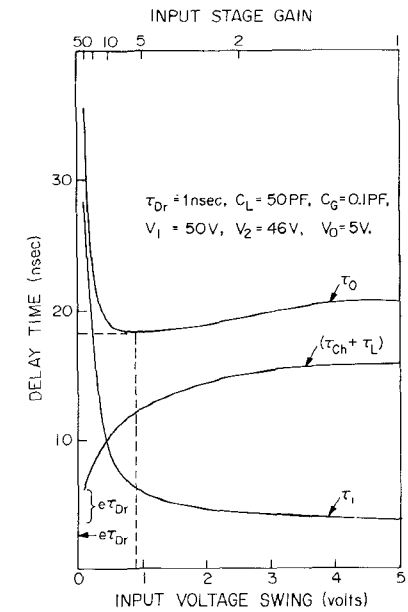

Fig. 9. Delay time versus line voltage swing V_i and input-stage gain G for a depletion-load push-pull driver chain driving 50-pF load and a regenerative balanced strobed-latch input stage.

gain by a factor of 3 from the optimum value increases the total delay time τ_D by about 50 percent. Irrespective of the line-to-gate capacitance C_L/C_G, the minimum transmission delay time τ_D on the large capacitance line is achieved with a driver-chain fan-out f equal to e and an input stage of sensing delay τ_i, half the delay per stage of the driver chain ($e\tau_{Dr}$).

B. Strobed-Latch Input Stage

For the strobed-latch input stage in Fig. 8 the latching delay time τ_i is inversely proportional to V_i with an optimum latching waveform and no off-side conduction [3] (as shown in Appendix B). The delay times associated with transmission on the high capacitance path with such an input stage are given by

$$\tau_i = \tau_0 \left(\frac{V_1}{V_i} + \frac{V_2}{V_{\text{th}}} \right)$$

$$(\tau_{\text{ch}} + \tau_L) = e\tau_{\text{Dr}} \ln \frac{C_L}{C_G} \frac{V_i}{V_o}$$

$$\tau_D = e\tau_{\text{Dr}} \ln \frac{C_L}{C_G} \frac{V_i}{V_o} + \tau_0 \left(\frac{V_1}{V_i} + \frac{V_2}{V_{\text{th}}} \right). \tag{32}$$

The delay times are plotted in Fig. 9 for a strobed input latch with the following parameters:

$$C_S = 0.1 \text{ pF} \quad C_g = 0.03 \text{ pF} \quad \frac{W}{L} = \frac{15}{5} \quad \frac{W_{el}}{L_{el}} = \frac{12}{3.8}$$

$$f = 0.77 \quad t_{0x} = 700 \text{ Å} \quad p = 12.6 \times 10^{-6} \text{ A/V}^2$$

$$\tau_0 = 0.05 \text{ ns} \quad V_1 = 50 \text{ V} \quad V_{\text{th}} = 0.7 \text{ V} \quad V_2 = 46 \text{ V}$$

$$V_o = 5 \text{ V} \quad \tau_{\text{Dr}} = 1 \text{ ns} \quad C_L = 50 \text{ pF} \quad C_G = 0.1 \text{ pF}.$$

The total delay time has a minimum at

$$V_{i/\min} = \frac{\tau_0}{e\tau_{\text{Dr}}} V_1, \tag{33}$$

where the delay times are given by

$$\tau_{i|\min} = e\tau_{Dr} + \tau_0 \frac{V_2}{V_{th}}$$

$$(\tau_{ch} + \tau_L)_{\min} = e\tau_{Dr} \ln \frac{C_L}{C_G} \frac{\tau_0}{e\tau_{Dr}} \cdot \frac{V_1}{V_o}$$

$$\tau_{D|\min} = e\tau_{Dr}\left[1 + \ln\left(\frac{C_L}{C_G} \frac{\tau_0}{e\tau_{Dr}} \frac{V_1}{V_o}\right) + \frac{\tau_0}{e\tau_{Dr}} \frac{V_2}{V_{th}}\right]$$

$$G_{|\min} = \frac{V_o}{V_i} = \frac{V_o}{V_1} \frac{e\tau_{Dr}}{\tau_0} \tag{34}$$

Similarly, in this case the increase in the total delay time τ_D for a voltage swing on the high capacitance path larger than the optimum value is rather small. Also, minimum transmission delay τ_D across the high capacitance path is achieved with a sensing delay τ_i of the input stage comparable to the delay per stage of the driver chain $e\tau_{Dr}$.

IV. Sensing Signals on Large Capacitance Lines

In many cases, the driver circuit at one end of the line is limited by constraints that limit the driver optimization previously discussed. Such cases are often encountered in sensing signals from small cells of large memory arrays. We consider below how we may minimize the total delay time of signal transmission on a high capacitance path with a fixed drive source at one end by optimizing the gain of the input stage and the line voltage swing.

In Fig. 10, the output driver is represented by a fixed current source I_o which drives the large capacitance line C_L with a voltage swing equal to V_i. The input stage senses the input signal at the other end of the line and generates an output voltage V_o equal to the supply voltage. The total transmission delay time τ_D in this case is equal to the sum of the sensing delay time τ_i of the input stage and the line delay time τ_L associated with the charging and discharging of the line capacitance C_L. Using (7) and (9), the delay time τ_D is given by

$$\tau_D = \tau_0 f(V_i) + T_o \frac{V_i}{V_o}. \tag{35}$$

If the input-stage delay τ_i is given by (20), the minimum delay time occurs at

$$G_{|\min} = \left[\frac{\tau_0}{n\alpha\tau_0}\right]^{1/(n+1)}$$

$$V_{i|\min} = V_o \left[\frac{n\alpha\tau_0}{\tau_0}\right]^{1/(n+1)}$$

$$\tau_{i|\min} = \frac{\tau_{L|\min}}{n}. \tag{36}$$

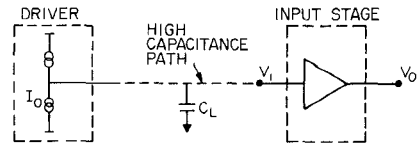

Fig. 10. Fixed driver drives a high capacitance load C_L. Input stage receives input signal V_i to generate output voltage V_o.

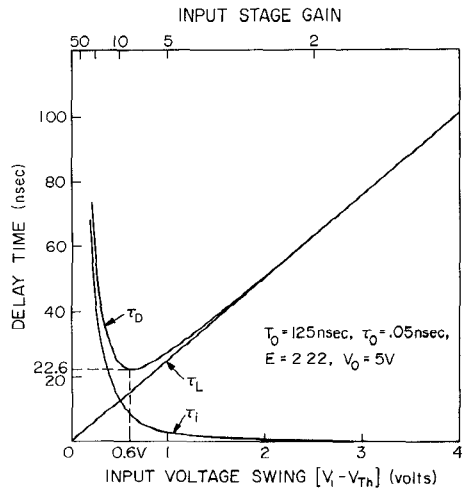

Fig. 11. Delay times versus line voltage swing V_i and input-stage gain G for a fixed driver driving a large capacitance load with a drive-time constant T_0 = 125 ns, and a depletion-load-inverter input stage.

The minimum delay time $\tau_{D|\min}$ for transferring the signal across the high capacity path is given by

$$\tau_{D|\min} = \left[1 + \frac{1}{n}\right]\tau_{L|\min} = \left[1 + \frac{1}{n}\right]\tau_0 \left[\frac{\tau_0 \alpha n}{\tau_0}\right]^{1/(n+1)}.$$

We consider below two numerical examples for a single-ended depletion-load-inverter input stage and a differential regenerative strobed-latch input stage.

A. Depletion-Load-Inverter-Input Stage

For the depletion-load-inverter input stage in Fig. 6, the input delay time is given by

$$\tau_i = \tau_0 E \frac{V_o^2}{(V_i - V_{th})^2}. \tag{37}$$

Assuming the voltage swing on the high capacitance line C_L is between V_i and V_{th}, the total delay time τ_D reduces to

$$\tau_D = \tau_0 E \frac{V_o^2}{(V_i - V_{th})^2} + T_o \frac{(V_i - V_{th})}{V_o}. \tag{38}$$

In Fig. 11, τ_i, τ_L, and τ_D are plotted for the following parameters:

$L = 4\ \mu m$ $\mu_{eff} = 500\ cm^2/V \cdot s$ $(V_o - V_{th}) = 4\ V$

$\tau_0 = 1/20\ ns$ $E = 2.2$ $C_L = 1\ pF$ $I_o = 40\ \mu A$

$T_o = 125\ ns.$

τ_D has a minimum at

$$(V_i - V_{th}) = \left[\frac{2\tau_0 E}{T_o}\right]^{1/3} V_o$$

where the values of τ_i, τ_L, τ_D, and G are given by

$$\tau_{i|min} = \tau_0 \left[\left(\frac{T_o}{2\tau_0}\right)^2 E\right]^{1/3}$$

$$\tau_{L|min} = 2\tau_{i|min}$$

$$\tau_{D|min} = 3\tau_{i|min}$$

$$G_{|min} = \left[\frac{T_o}{2\tau_0 E}\right]^{1/3}. \tag{39}$$

In Fig. 11, a minimum of τ_D at 22 ns exists at an input voltage swing of 0.6 V, which is about a factor of 5 less than the delay time τ_D with full supply voltage swing. The minimum delay time is achieved with the input-stage delay time τ_i equal to half the line delay time τ_L.

B. Strobed-Latch Input Stage

For the strobed-latch input stage with an optimum latching waveform and no off-side conduction, the total delay time is given by

$$\tau_D = \tau_0\left(\frac{V_1}{V_i} + \frac{V_i}{V_{th}}\right) + T_o \frac{V_i}{V_o}. \tag{40}$$

The delay times are plotted in Fig. 12 for a strobed input latch with the following parameters:

$$C_S = 0.1 \text{ pF} \quad C_g = 0.03 \text{ pF} \quad \frac{W}{L} = \frac{15}{5} \quad \frac{W_{el}}{L_{el}} = \frac{12}{3.8}$$

$$f = 0.77 \quad t_{0x} = 700 \text{ Å} \quad \tau_0 = 0.05 \text{ ns} \quad V_1 = 50 \text{ V}$$

$$V_{th} = 0.7 \text{ V}, \quad V_2 = 46 \text{ V} \quad V_o = 5 \text{ V} \quad C_L = 1 \text{ pF}$$

$$I_o = 40\ \mu\text{A} \quad T_o = 125 \text{ ns}.$$

τ_D has a minimum at

$$V_{i|min} = \sqrt{\frac{\tau_0}{T_0}}\, V_o V_1$$

where the values of τ_i, τ_L, τ_D, and G are given by

$$\tau_{i|min} = \tau_0\left[\sqrt{\frac{T_0}{\tau_0}\frac{V_1}{V_o}} + \frac{V_{th}}{V_2}\right]$$

$$\tau_{L|min} = \tau_0 \sqrt{\frac{T_0}{\tau_0}\frac{V_1}{V_o}}$$

$$\tau_{D|min} = \tau_0\left[2\sqrt{\frac{T_0}{\tau_0}\frac{V_1}{V_o}} + \frac{V_{th}}{V_2}\right]$$

$$G_{|min} = \sqrt{\frac{\tau_0}{T_0}\frac{V_1}{V_o}}. \tag{41}$$

In Fig 12 the minimum delay time τ_D is 18.5 ns for $V_i = 0.3$ V. Similarly, in this case the minimum total delay time to transmit the signal across the large capacitance line is achieved with a line voltage swing and input-stage gain such that the sensing delay τ_i of the input stage is comparable to the line delay time τ_L.

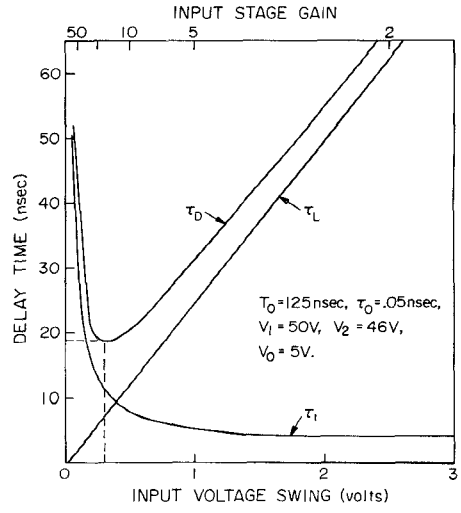

Fig. 12. Delay time versus line voltage swing V_i and input-stage gain G for a fixed driver driving a large capacitance load with a drive-time constant T_0 = 125 ns and a regenerative balanced strobed-latch input stage.

V. Conclusions

We have examined how to minimize the delay time associated with the transmission of signals across large capacitance paths by optimizing the driving and sensing circuits. In our analysis we have considered the design of the driver and sensing circuits in general terms by optimizing the fan-out of the driver-stages chain, the gain of the input sensing circuit, and the path voltage swing.

For driving large capacitive loads, we have found that the drive delay time of a chain of successive drivers has a broad minimum at a fan-out factor f around e, the base of the natural logarithms. The delay times of each stage of the driver chain are equal to $e\tau_{Dr}$, where τ_{Dr} is the delay time of a driver driving a similar driver. This is a result of the exponential growth of the drive capabilities of the successive stages of the driver chain. At this minimum, the number of stages in the driver chain is equal to the natural logarithm of the load capacitance to the gate capacitance C_L/C_G. The minimum driver-chain delay time τ_{ch} is equal to the delay per stage of the driver chain $e\tau_{Dr}$ times the number of stages $\ln(C_L/C_G)$. For fan-out factor f larger than e, the relative delay time penalty is relatively small.

Minimization of the total transmission time on a large capacitance path, in cases where the fan-out factor of the driver chain, the gain of the input sensing stage, and the path voltage swing can be optimized, have been examined. Minimum total delay is achieved with a driver chain of fan-out f equal to e and an input stage with an input sensing delay related to the delay per stage of the driver chain according to the delay-time gain characteristic of the input stage. Irrespective of the ratio of the path-to-gate capacitance, the total delay time has a broad minimum for line voltage swings above the optimum swing, but a rather sharp minimum for input-stage gain above the optimum gain. For line voltage swings above the optimum value, the driver chain and line delay times are dominant and

the total delay times increase logarithmically with the line voltage swing. Therefore, in such cases full supply voltage swing on the high capacitance line provides better noise immunity against interferring signals with a relatively small time penalty. Delay times for push-pull depletion-load-driver stages with a single-ended depletion-load-inverter input stage and with a balanced regenerative strobed latch have been analyzed. For a single-ended depletion-load-inverter input stage (delay time $\tau_i \alpha^{al}$ 1/(gain)^2), the minimum total delay is achieved with an input-stage delay τ_i equal to one-half the delay per stage of the driver chain $e\tau_{Dr}$. For a regenerative balanced strobed-latch input stage (delay time $\tau_i \alpha^{al}$ 1/(gain)), minimum delay time occurs when the input-stage delay τ_i is comparable to the delay per stage of the driver chain.

Minimization of the total transmission time on a large capacitance path in cases where the driver is fixed and the line voltage swing and the gain of the input stage can be optimized, have been presented. Cases of fixed drivers of large capacitance lines are encountered in sensing stored information from memory cells of large arrays. Minimum total delay is achieved with a line voltage swing and an input stage such that the line delay time is related to the input sensing delay according to the delay-time gain characteristics of the input stage. For a single-ended depletion-load-inverter input stage (delay time $\tau_i \alpha^{al}$ 1/(gain)^2), the minimum total delay is achieved at a line voltage swing and input-stage gain such that the input-stage delay time τ_i is half the line delay time τ_L. For a differential regenerative balanced strobed-latch input stage (delay time $\tau_i \alpha^{al}$ 1/(gain)), the minimum total delay occurs when the input-stage delay τ_i is comparable to the line delay time τ_L. Deviations of the gain and line voltage swing by a factor of 2 from the minimum may increase the total delay time by as much as 75 percent for the examples considered in this paper.

In general, we may conclude that a minimum transmission time of signals in a system consisting of several stages is achieved when the delay times of the different stages are comparable. For the case of driving and sensing signals from large capacitance paths, minimum delay time is achieved when the delay times of the successive stages of the driver chain, the high capacitance path, and the input sensing stage are comparable.

Appendix A

The output of the input-stage circuit can be represented by a source voltage V_s that corresponds to the amplified undelayed input voltage V_i to the stage and a delay τ_i provided by a simple RC circuit as shown in Fig. 13(a). We show below that if the input-stage delay τ_i is less than the line delay τ_L, the total delay τ_D is approximately equal to the sum of the input stage delay τ_i and the line delay τ_L.

In Fig. 13(b) the responses of the input-stage equivalent circuit to a step, a ramp, and a sinusoidal input are shown. For a step input

$$t>0 \quad V_S = V_0 \quad V_{out} = V_0 [1 - \exp(-t/\tau_i)]. \tag{A-1}$$

For a ramp input

$$t>0 \quad V_S = \frac{t}{\tau_L} V_0 \quad V_{out} = \frac{(t-\tau_i)}{\tau_L} + \frac{V_0}{\tau_L} \exp(-t/\tau_i). \tag{A-2}$$

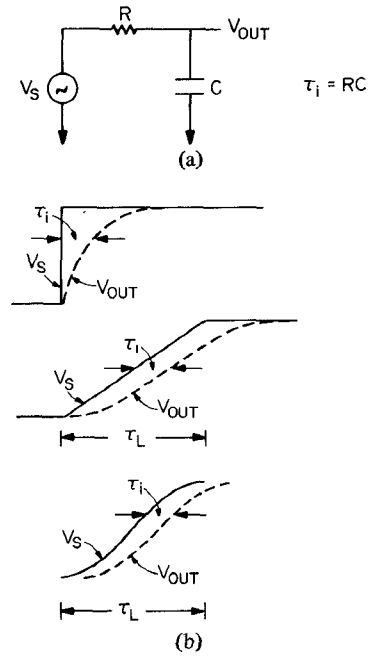

Fig. 13. (a) Equivalent circuit of the input sensing stage. (b) The output responses of the input stage to a step, a ramp, and a sinusoidal input.

If $\tau_L > \tau_i$, then

$$V_{out} \simeq \frac{(t-\tau_i)V_0}{\tau_i}. \tag{A-3}$$

For a sinusoidal input

$$t>0 \quad V_S = \frac{V_0}{2}\left[1 - \cos\frac{\pi t}{\tau_L}\right] \quad V_{out} = \frac{V_0}{2} \cdot \left[1 - \cos\frac{\pi(t-\theta)}{\tau_2}\right] \quad \theta = \frac{\tau_L}{\pi}\tan^{-1}\frac{\pi\tau_i}{\tau_L}. \tag{A-4}$$

If $\tau_L > \tau_i$, then

$$V_{out} \simeq \frac{V_0}{2}\left[1 - \cos\frac{\pi(t-\tau_i)}{\tau_L}\right]. \tag{A-5}$$

From (A-3) and (A-4), it is apparent that for $\tau_L > \tau_i$ the output voltage V_{out} is delayed from the amplified undelayed input voltage V_s by the input stage delay τ_i. Thus, in general, if $\tau_i < \tau_L$, the total delay τ_D is the sum of the line delay τ_L and the input-stage delay τ_i

$$\tau_D \simeq \tau_L + \tau_i. \tag{A-6}$$

Appendix B

Dynamic MOS regenerative latch sensors, as in Fig. 8, can amplify a small initial imbalance V_i between the two internal nodes D and G to a voltage difference comparable to the initial power-supply voltage V_0. For smaller initial voltage imbalance the latch-up time is, in general, larger. For any given initial imbalance V_i, there is an ideal latching waveform that minimizes the latch time [3]. The initial imbalance represents the sum of the real voltage imbalance and any threshold imbalance of the MOS crosscoupled transistor pair. The general shape of the optimum latching waveform is shown in Fig. 8. It con-

sists of an initial step followed by a ramp of gradually increasing slope to the final voltage value.

The internal latch nodes D and G are precharged to V_0. The input voltage introduces an imbalance V_i on nodes D and G. To minimize threshold imbalances and reduce power dissipation, the flip-flop load devices are turned off during latchup. The latch-up waveform $V_s(t)$ can be selected such that no current flows through the off-side during latchup to maximize the final latched imbalance. However, coupling capacitances to the off-side lower its final voltage and lowers the conduction of the on transistor, thus increasing the latching time. The optimum latching waveform [3] consists of two portions given by

$$V_s(t) = V_0 - V_{th} - \frac{V_i - t/\tau}{1 - t/\tau} \quad \text{for} \quad t < t_{sat} \tag{B-1}$$

and

$$V_s(t) = V_0 + V_{in} - V_{th} - \frac{V_{th}}{2f}\{3 + \exp[(t - t_{sat})/\tau_1]\} \quad \text{for} \quad t > t_{sat} \tag{B-2}$$

where

$$f = \frac{C_s}{(C_s + C_g)}$$

$$\tau = \frac{2C_s}{\beta f^2 V_i}$$

$$\tau_1 = \frac{C_s}{\beta f V_{th}}$$

$$t_{sat} = \frac{2C_s(V_{th} - fV_i)}{\beta f^2 V_{th} V_i} \tag{B-3}$$

where C_g, β, and V_{th} are the gate capacitance, current factors, and threshold voltages of T_1 and T_2; and C_s is the capacitance of latch nodes D and G. The latch time τ_i is given by

$$\tau_i = \tau_0\left(\frac{V_1}{V_i} + \frac{V_2}{V_{th}}\right) \tag{B-4}$$

where τ_0 is the transit time across gate and is given by

$$\tau_0 = \frac{C_g}{\beta(V_G - V_{th})} = \frac{L^2}{\mu(V_G - V_{th})}$$

$$V_1 = \frac{2C_s}{C_g}\frac{(V_{th} - fV_i)}{V_{th}}\frac{V_0}{f^2}$$

$$V_2 = \frac{C_s}{C_g}\frac{V_0}{f}\ln\left[\frac{f(V_0 \pm V_i - V_{th}) - V_{th}/2}{V_{th}/2}\right]. \tag{B-5}$$

Thus the total latch τ_i is approximately inversely proportional to the initial unbalance V_i.

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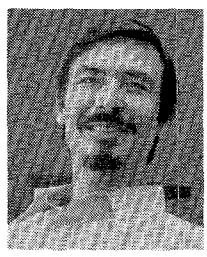

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